Remarks

Reconsideration of the application and allowance of all pending claims are respectfully requested. **Applicants respectfully request consideration of the remarks below in light of the newly cited reference.** Claims 1-65 remain pending.

In the Office Action, dated November 12, 2004, claims 1-6, 8, 9, 13-18, 20-26, 28, 29, 33-38, 40-50, 52, 53, 57-62, 64, and 65 are rejected under 35 U.S.C. 102(b) as being anticipated by Brent et al. (U.S. Patent No. 5,459,864); and claims 7, 19, 27, 39, 51 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brent in view of Dievendorff et al. (European Patent Application 0280773 A2). Applicants respectfully, but most strenuously, traverse these rejections for the reasons below.

In one aspect, applicants' invention is directed to a processor taking over one or more queues of another processor of a communications environment. That is, for one reason or another, the queues of one processor are inaccessible, and thus, another processor takes over one or more of those queues. The queues being taken over are memory resident queues. That is, they are queues that reside in, for instance, local memory of a processor, as opposed to DASD or some other storage unit. The queues are, therefore, volatile by nature. For example, if a processor is inactive, then the queues in memory are inaccessible and lost.

Previously, in order to access inaccessible memory resident queues, those queues would need to be rebuilt by the processor that owned those queues. However, in accordance with an aspect of the present invention, those queues are now taken over by at least one other processor by moving one or more of the queues (e.g., the contents of the queues) to the other processor. The queues, once taken over, are then resident in the other processor's memory, and no longer resident in the first processor's memory.

In one particular example, applicants claim a method of switching queue ownership (e.g., independent claim 1). The method includes, for instance, obtaining an indication that a queue is to be taken over, the queue being resident in memory of a first processor; and moving the queue from the first processor to a second processor, the queue to be resident in memory of the second processor and not resident in memory of the first processor. Thus, in applicants' claimed invention, when a queue is moved from one processor to another processor, the queue (e.g., the contents of that queue) is no longer resident in memory of the processor from which it is moved.

Instead, it is resident in the memory of the processor to which it is moved. This is very different from the teachings of Brent.

In Brent, there is no moving of a queue from the memory of one processor to the memory of another processor, since in Brent, the queues are maintained in shared memory. This is described in various sections of Brent. For instance, in FIG. 2 of Brent, there is depicted a common control and data bus indicating that the multiple QOPs have access to the same system memory. Further, at Col. 10, lines 41-44, it is indicated that each QOP has a queue header which is at a known address so that is accessible by all CPUs and other QOPs. This address is a memory address. Since the address is accessible by all CPUs and QOPs, applicants respectfully submit that it is shared memory. Moreover, at Col. 8, lines 8-10, there is a description of how queue elements (QEs) are chained into a particular queue using the address of the QE. Once again, this address is a memory address. As yet a further example, the paragraph at Col. 17, lines 64-67 and Col. 18, lines 1-11 of Brent describes the recovery process of moving QEs from the error-QOP to the recovery-QOP. It mentions enqueuing the QEs from the failing QOP into the recovery QOP. From above, it is known that this queuing involves chaining with memory addresses. Thus, it is shared memory that enables one QOP to be able to chain in the QEs from another QOP.

In Brent, the queues themselves for the multiple processors reside in the same physical memory, and thus, there is no moving of the queues from one memory to another memory. That is, there is no description, teaching or suggestion in Brent of moving a queue from a first processor to a second processor, in which the queue is resident in memory of the second processor and not resident in memory of the first processor, as claimed by applicants. In contrast, in Brent, the queues remain in memory shared by both processors. For at least this reason, applicants respectfully submit that their invention is patentable over Brent.

Support for the rejection is indicated at Col. 1, lines 18-21 and Col. 5, lines 39-44 and 49-52 of Brent. However, applicants respectfully submit that a careful reading of these sections fails to describe, teach or suggest one or more aspects of applicants' claimed invention. For example, there is no teaching in any of those cited sections of moving a queue from a first processor to a second processor, in which the queue is resident in memory of the second processor and not resident in memory of the first processor. This is not taught in Brent. The sections cited merely describe that automatic load balancing among queue processors is provided and that work may be redistributed to other processors through the subsystem workload

balancing process. There is no description in any of those sections of moving a queue, such that it is no longer resident in one memory, but resident in another. The teaching of load balancing in which work is performed by another processor is not equivalent to moving a queue from one memory to another memory. In Brent, residency of a queue need not be moved, since the processors share memory. The only movement in Brent is the responsibility for performing work. There is no moving of a queue from a first processor to a second processor, in which the queue is resident in memory of the second processor and not resident in memory of the first processor, as claimed by applications. Thus, applicants respectfully submit that their claimed invention is not described, taught or suggested in Brent.

Moreover, applicants respectfully submit that Brent does not describe, teach or suggest switching ownership of a queue. Instead, in Brent, only selected queue elements are processed by another processor. Other queue elements remain on the queue and are not so processed. Since only selected queue elements are processed by other processors, at the most it can be said is that ownership of selected queue elements is switched and not ownership of the queue, itself.

Further, applicants respectfully submit that the teaching in Brent of detecting a failure signal from a processor is not equivalent to obtaining an indication that a queue is to be taken over, as claimed by applicants. Applicants respectfully submit that just because there is a failure that does not necessarily mean that queue ownership is to be taken over. In contrast, in applicants' claimed invention, when a queue is to be taken over, a particular indication is provided. The mere failure is not an indication that a queue is to be taken over. There are many situations in which a processor fails, but the queue ownership is to remain with that processor. Thus, applicants respectfully submit that the mere teaching of detecting a failure signal is not the same as obtaining an indication that a queue is to be taken over.

For all of the above reasons, applicants respectfully submit that claim 1, as well as the other independent claims are patentable over Brent. Further, applicants respectfully submit that the dependent claims are patentable for the same reasons as the independent claims, as well as for their own additional features.

As one particular example, in dependent claim 6, applicants claim that the rebuilt version of the queue is written to the checkpoint of the queue. Applicants respectfully submit that this feature is not taught or suggested in Brent. In contrast to Brent, in applicants' invention, the messages are guaranteed persistent. Thus, the contents of a recovered queue are written out to a

persistent storage medium, so that in the event that all processors encounter a failure, the contents of the queue will be fully recoverable from the persistent storage medium. In Brent, the queue elements are not persistent. If all the QOPs fail, then all the queues and all of the QE contents are lost. Brent describes that if the last active processor is removed, then there are no remaining processors to distribute the queue elements amongst, and this implies that the queues must be lost (see, Col. 5, lines 49-52; Col. 6, lines 33-37). Thus, applicants respectfully submit that Brent fails to describe, teach or suggest applicants' claimed element of writing the rebuilt version of the queue to the checkpoint of the queue, and therefore, respectfully request an indication of allowability for this claim and any similar claims.

As a further example, in dependent claim 7, applicants recite that at least a portion of a recovery log used in rebuilding a queue is processed in reverse order. This claim is rejected based on a combination of Brent and Dievendorff. Applicants respectfully submit, however, that Dievendorff does not overcome the deficiencies of Brent and that Dievendorff does not teach the processing of a queue in reverse order, as indicated in the Office Action. In contrast to applicants' claimed invention, Dievendorff explicitly states, "[T]he log is read forward from that point..." (see, e.g., page 5, lines 8-10, lines 28-30, lines 51-55). Dievendorff does not teach or suggest processing a portion of a recovery log in reverse order. Instead, Dievendorff teaches the opposite. Thus, applicants respectfully submit that Dievendorff, either alone or in combination with Brent, does not teach or suggest applicants' claimed invention.

Based on the foregoing, applicants respectfully submit that all pending claims are patentable over Brent, either alone or in combination with Dievendorff. Applicants gratefully acknowledge the indication of allowability of claims 10-12, 30-32 and 54-56, if rewritten in independent form. At this time, applicants have not rewritten those claims in independent form, since applicants believe that the claims from which they depend are patentable for the reasons described above.

Should the Examiner wish to discuss this case with applicants' attorney, please contact applicants' attorney at the below listed number.

Respectfully submitted,

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